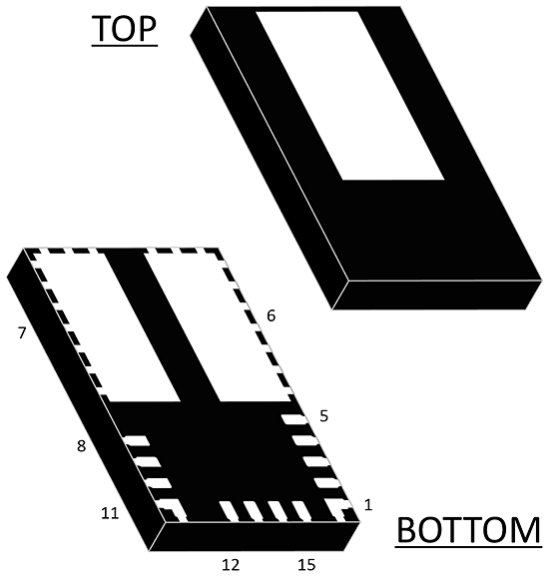
GR-10Y005ZQ: Self-Protected 100V GaN with Integrated Driver

Description

The GR-10Y005ZQ is a Gallium Nitride (GaN) FET with integrated driver. The device features a 100V rated GaN FET driven by an optimized high-frequency GaN FET driver. The GR-10Y005ZQ incorporates an high-side level shifter and bootstrap circuit. This integration allows GR-10Y005ZQ unit to form a half-bridge topology without the need for external level-shifting circuit. The driver and the GaN FET are mounted using Flip-chip bond packaging technology, resulting in minimized package parasitic elements.

GR-10Y005ZQ



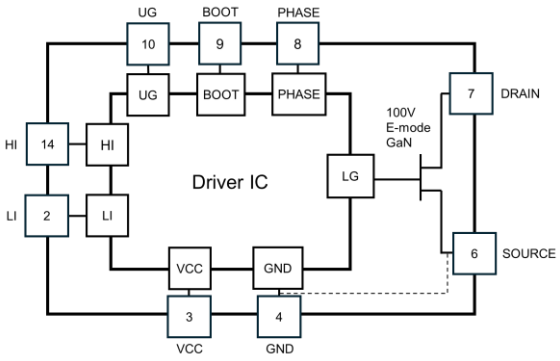
Key Specifications

Part Number	GR-10Y005ZQ
V_{DSS}, min.	100V
$R_{DS(ON)}$, typ.	3.5mΩ
Package	QFN-4.0x6.5x0.7

Features

- Gate drive voltage compatibility
- High operating frequency
- Over temperature protection
- Short circuit protection
- 20 ns typical delay time

Simplified Function Block



Applications

- Switch Mode Power Supplies (SMPS)
- AC-DC/ DC-DC Converters
- Motor/Robot Drives

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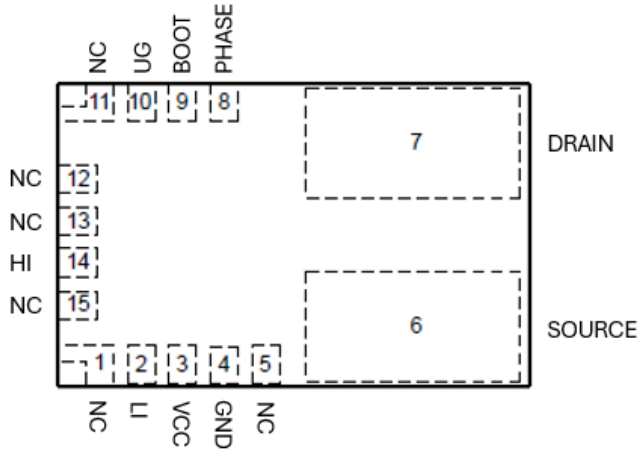
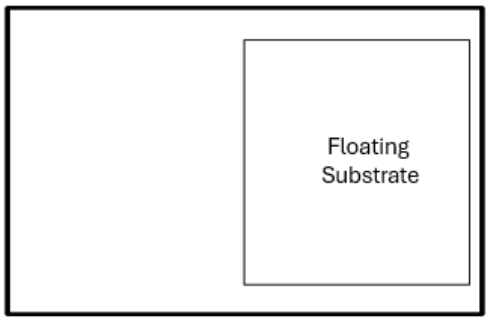
1- Pin Configuration and Description



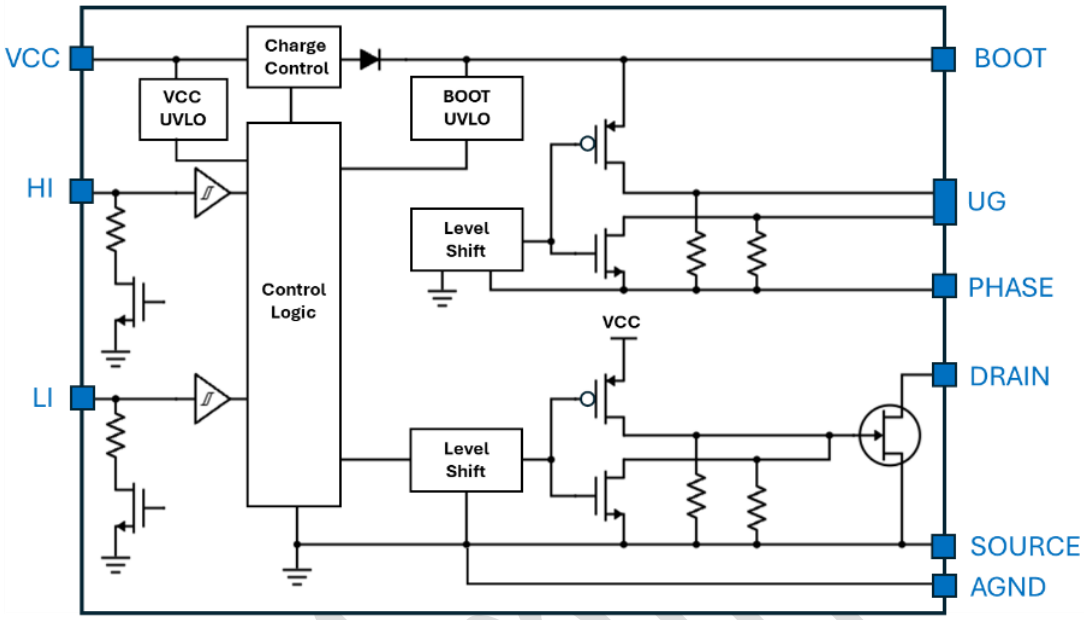
Transparent Top View
(Pin Definition)



Top View
(Exposed GaN Die Si Substrate)

Pin Name	Pin No.	I/O/P	Pin Function
NC	1, 5, 11-13, 15	-	Not connection. Do not connect to any circuit. It is recommended that these pins be left floating.
LI	2	I	Low-side driver PWM input.
VCC	3	P	Supply voltage for the IC. This pin provides bias voltage for the IC. Connect a 1uF capacitor between VCC to GND and place it as close to the pin as possible.
GND	4	G	Ground return.
SOURCE	6	P	Source of E-mode GaN FET. Internally connected to GND.
DRAIN	7	P	Drain of the E-mode GaN FET.
HS	8	P	**Switch Node.** Connect to the source of high-side FET and bootstrap capacitor terminal.
BOOT	9	P	**High-Side Gate Driver Bootstrap Rail.** The bootstrap capacitor provides the charge to turn on the high-side GaN FET. Connect a minimum 0.1uF capacitor C_{BOOT} between BOOT to PHASE pin. The C_{BOOT} must be placed as close to the BOOT and PHASE pins as possible.
UG	10	O	Level shifted high-side gate driver control output.
HI	14	I	High-Side Driver PWM Input.

2- Functional Block Diagram



3- Functional Description

3.1 Overview

The GR-10Y005ZQ is a 100V Gallium Nitride (GaN) FETs with integrated both high-side and low-side driver, which is suitable in synchronous buck or half bridge configuration. This device supports the half-bridge / synchronous buck converter application with switch node voltage up to 100V DC or pulsed 120V, without an additional level shifter.

GR-10Y005ZQ is designed to have short propagation delay time and output rise/fall time, which makes this device suitable for fast switching application.

The use of GaN FETs drastically improves power conversion efficiency due to their zero reverse recovery loss and extremely low input capacitance (CISS) and output capacitance (COSS). Furthermore, the driver and the GaN FET are integrated into a package designed without bond wires, effectively minimizing parasitic inductance.

By integrating a more user-friendly interface, this device makes the superior performance of discrete GaN FETs more accessible. It is the perfect fit for applications demanding high frequency and high efficiency in a compact footprint. The GR-10Y005ZQ device is available in a 6.5mm x 4mm x 0.90mm lead-free package and can be easily mounted on PCBs.

3.2 Under Voltage Lockout (UVLO)

The GR-10Y005ZQ features internal UVLO circuitry to monitor both the VCC and BOOT-PHASE voltage separately. If the VCC voltage falls below the its POR threshold, the device turns off all outputs and ignores both the HI and LI PWM inputs. If the VCC voltage is above its POR threshold VCCRTH while BOOT-PHASE is below its POR threshold VBOOTPORL, the device turns off only high-side FETs (UGH=Open, UGL=ON), but the LG responds per LI input and ignores HI PWM inputs. Only when the VCC voltage and BOOT-PHASE voltage are all above their POR threshold, the device drives the FETs per HI and LI PWM inputs.

3.3 Bootstrap Clamp

Due to the characteristics of enhancement mode GaN FETs, the source to drain voltage is usually higher than a diode forward voltage where the low-side GaN FET operates in body-diode mode. This will cause negative voltage on PHASE pin during the switching dead time. The source to drain voltage can be in the range of 1.5 V to 2.5 V. The device utilizes floating bootstrap technique to supply power to the high-side driver. The negative PHASE voltage can lead to an overcharging phenomenon to the bootstrap capacitor, causing higher voltage across the bootstrap capacitor. The overcharging of bootstrap capacitor causes an issue of the applied gate-to-source voltage exceeding its maximum rating and then damages the high-side GaN FET. Therefore, the uP1969 solves this issue with an internal switch to disconnect the bootstrap diode from VCC when low-side GaN FET is turned off.

4- Absolute Maximum Rating

Specification	MIN	MAX	Unit
Drain to Source	-	100	V
Drain to Source (5ms pulses at 150°C)	-	120	V
BOOT to AGND	-0.3	$V_{PHASE}+V_{CC}$	V
PHASE to AGND (DC)	-0.3	100	V
PHASE to AGND (<25ns)	-5	105	V
HI to AGND	-0.3	6.6	V
LI to AGND	-0.3	6.6	V
VCC to AGND	-0.3	6.6	V
BOOT to PHASE	-0.3	6.6	V
BOOT to PHASE (<25ns)	-0.3	7.0	V
IOUT, DRAIN/SOURCE pins (Continuous), TJ = 125℃	-	68	A
Junction Temperature, T_J	-40	150	℃
Storage Temperature, T_S	-40	150	℃

5- Specification

5.1 Electrical Characteristics

(Vcc=VBOOT=5V, VGND=VPHASE=0V, T_J=25℃, unless otherwise noted)

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
GaN FET on-resistance	$R_{DS(ON)}$	LI=V_{CC}=5V, HI=0V, I(DRAIN-SOURCE)=16A, T_J= 25℃	-	3.5	4.2	mΩ
GaN 3rd quadrant conduction drop	V_{SD}	I_{SD} = 500 mA, V_{CC} = 5 V, HI = LI = 0V	-	1.5	-	V
Leakage from DRAIN to SOURCE when the GaN FET is off	$I_{L-DRN-SRC}$	DRAIN = 80V, HI = LI = 0V, V_{CC} =5V, T_J=25℃	-	1	20	μA
Output Capacitance of GaN FET	C_{OSS}	V_{DS}=50V, V_{GS}= 0V (HI = LI = 0V)	-	425	586	pF
Output Capacitance of GaN FET – Energy, Related	$C_{OSS(ER)}$	V_{DS}=0 to 50V, V_{GS}= 0V (HI = LI = 0V)	-	482	-	pF
Output Capacitance of GaN FET – Time, Related	$C_{OSS(TR)}$	V_{DS}=0 to 50V, V_{GS}= 0V (HI=LI= 0V)	-	603	-	nC
Total Gate Charge of GaN FET	Q_G	V_{DS}=50V, I_D= 16A, VGS= 5V	-	8.5	9.8	nC
Gate to Drain Charge of GaN FET	Q_{GD}	V_{DS}=50V, I_D= 16A		0.9		nC

Parameter	Symbol	Test Condition	MIN	TYP	MAX	Unit
Gate to Source Charge of GaN FET	Q_{GS}	V_{DS}=50V, I_D= 16A		3.1		nC
Output Charge	Q_{OSS}	VDS=50V, V_{GS} = 0 V		31	38	nC
Source to Drain Reverse Recovery Charge	Q_{RR}	Not including internal driver bootstrap diode		0		nC
V_{CC} Quiescent Current	I_{CCQ}	LI = HI = 0V, VCC = 5V		120	200	uA
V_{CC} Operating Current	I_{CCO}	F_{SW}=500kHz, C_{LOAD}=0nF		1.5	2.5	mA
BOOT Quiescent Current	I_{BOOTQ}	LI = HI = 0V, VCC = 5V, C_{LOAD}=0nF		0.1	0.12	mA
BOOT to GND Leakage Current	I_{QBOOTG}	HI=LI=0V,V_{PHASE}=V_{BOOT}=100V		0.3		uA
BOOT Operating Current	I_{HBO}	F_{SW}=500kHz, C_{LOAD}=0nF		1.5	2.5	mA
Propagation delay: HI Rising	t_{HIPLH}	LI=0V, VCC=5V, HB-HS=5V, VIN=48V		30	40	ns
Propagation delay: HI Falling	t_{HIPHL}	LI=0V, VCC=5V, HB-HS=5V, VIN=48V		30	40	ns
Propagation delay: LI Rising	t_{LPLH}	C_{LOAD}=1nF, LI rising to LG rising		30	40	ns
Propagation delay: LI Falling	t_{LPHL}	C_{LOAD}=1nF, LI rising to LG		30	40	ns
Delay Matching: LI high & HI low	t_{MON}			1.5	6	ns
Delay Matching: LI low & HI high	t_{MOFF}			1.5	6	ns
High-Level Input Voltage Threshold	V_{IH}		2.3			V
Low-Level Input Voltage Threshold	V_{IL}				0.5	V
Input Voltage Hysteresis	V_{IHYS}			400		mV
Input pull down resistance	R_{IN}			200		kΩ
Minimum Input Pulse Width That Changes the Output	T_{PW}			10		ns
Minimum Gate Output Pulse	T_{GATE_MIN}			15		ns
V_{CC} Rising edge threshold	V_{CC}	Rising	3.8	4	4.2	V
V_{CC} UVLO threshold hysteresis	$V_{CC(hyst)}$			0.3		V
BOOT POR Rising Threshold	$V_{BOOTPORH}$	$V_{BOOT-PHASE}$ Rising edge	2.5	3.4	3.9	V
BOOT POR Falling Threshold	V_{HBF}	$V_{BOOT-PHASE}$ Falling edge	2.3	3.2	3.7	V
BOOT POR Threshold Hysteresis	$V_{HB(hyst)}$			0.2		V
Low-Current forward voltage	V_{DL}	I_{VDD-HB} = 100μA		0.2	0.4	V
High current forward voltage	V_{DH}	I_{VDD-HB} = 100mA		0.9	1.2	V
Dynamic Resistance	R_D	$I_{VCC-BOOT}$ =1mA to 100 mA		8		Ω

Note 1: Guaranteed by design but not tested in production.

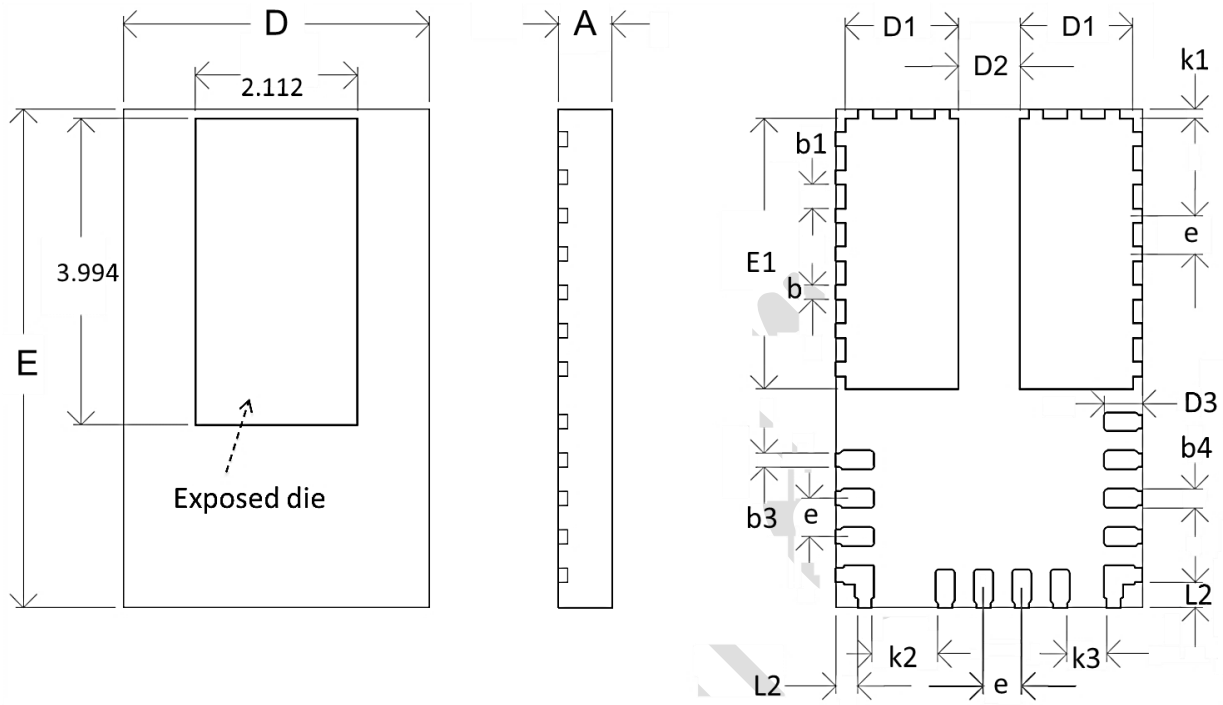
5.3 Thermal Information

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	34.5	°C/W
$R_{\theta JC}$	Junction-to-case (top) thermal resistance	0.45	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.9	°C/W
$R_{\theta JC(Bot)}$	Junction-to-case (Bottom) thermal resistance	3.3	°C/W

5.4 ESD Information

Symbol	Parameter	Value	Unit
HBM	Human Body Model (IC PIN)	±2k	V
CDM	Charged Device Model (IC PIN)	±1k	V

6- Package Outline Dimension



SYMBOL	DIMENSION (MM)			SYMBOL	DIMENSION (IN MM)		
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.
A	--	0.65	0.70	**b2**	0.08	0.18	0.28
D	3.90	4.00	4.10	**b3**	0.15	0.25	0.35
D1	1.375	1.475	1.575	**e**	0.40	0.50	0.60
D2	0.70	0.80	0.90	**L1**	0.185	0.285	0.385
D3	0.40	0.50	0.60	**L2**	0.135	0.235	0.335
E	6.40	6.50	6.60	**k1**	0.025	0.125	0.225
E1	3.425	3.525	3.625	**k2**	0.670	0.870	0.970
b	0.09	0.19	0.29	**k3**	0.420	0.520	0.620
b1	0.21	0.31	0.41				

7- Change Log

Version	Date	Description
01	November 2, 2025	Initial version

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